UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,642	05/01/2001	Luciano Lavagno	CA7012162001	6620

55497 7590 06/01/2009

VISTA IP LAW GROUP LLP
1885 Lundy Avenue
Suite 108
SAN JOSE, CA 95131

EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
06/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/847,642	LAVAGNO ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-22,33,34 and 36-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-22,33,34 and 36-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to a Request for Continued Examination filed April 6, 2009. No claims were canceled. Claims 61 - 64 were added. Claims 1 – 2, 4 – 22, 33 – 34 and 36 – 64 are pending. Claims 1 – 2, 4 – 22, 33 – 34 and 36 – 64 have been examined. Claims 1 – 2, 4 – 22, 33 – 34 and 36 – 64 are rejected. Claims 1 – 2, 4 – 22, 33 – 34 and 36 – 64 are allowable over the prior art of record.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 6, 2009 has been entered.

Response to Remarks

3. Regarding claims 1, 9, 41, 55 objected to:

   3.1. Applicant's claim amendments overcome the objections.

4. Regarding claims 1, 9, 16, 33, 41, 55 rejected under 35 USC § 112, second paragraph:

   4.1. The Examiner thanks the Applicant for the claim amendments, which overcome most of the rejections.

4.2. Applicant's claim amendments overcome most of the rejections; however, the amendments to claim 41 introduce a new rejection under 35 USC § 112, second paragraph, and continue to recite "the software simulation model" in lines 15 - 16, which appears to have insufficient antecedent basis.

5. Regarding claim 41 rejected under 35 USC § 112, first paragraph:

5.1. Applicant's arguments have been fully considered, but are not persuasive, as follows.

5.2. Regarding Applicant's arguments on pages 16 - 17, section II., subsection A: The Applicant essentially recites sections of the specification that allegedly support the claim. The Examiner respectfully disagrees as follows: The Applicant's recited portions of the specification do not appear to support disassembling a binary code into a simulation model. The specification appears to teach disassembling binary code into an assembly code module. The Examiner remarks that deleting the phrase, "by disassembling a binary code" may overcome the rejection. The Examiner remarks that several of the claims rejected under 35 USC § 112, first paragraph, may be mixing two different embodiments of the invention. Please also note the related new rejections of claim 41 below necessitated by the amendments.

6. Regarding claim 55 rejected under 35 USC § 112, first paragraph:

6.1. Applicant's arguments have been fully considered, but are not persuasive, as follows.

6.2. Regarding Applicant's arguments on pages 18 - 19, section II., subsection B: The Applicant essentially recites sections of the specification that allegedly support the claim. The Examiner respectfully disagrees as follows: The

Applicant's recited portions of the specification do not appear to support generating an assembler-level software simulation model by disassembling a binary code. The specification appears to teach disassembling binary code into an assembly code module. The Examiner remarks that deleting the phrase, "or by disassembling a binary code" may overcome the rejection.

7. Regarding claim 1 rejected under 35 USC § 112, first paragraph:

7.1. Applicant's arguments have been fully considered, but are not persuasive, as follows.

7.2. Regarding Applicant's arguments on pages 20 - 21, section II., subsection C: The Applicant essentially recites sections of the specification that allegedly support the claim. The Examiner respectfully disagrees as follows: The Applicant's recited portions of the specification do not appear to support disassembling a binary code into a software simulation model, nor by disassembling binary code into the optimized assembler code generated in a preceding limitation. The Examiner remarks that deleting the phrase, "by disassembling a binary code" may overcome the rejection.

8. Regarding claim 41 rejected under 35 USC § 112, first paragraph:

8.1. Applicant's arguments have been fully considered, but are not persuasive, as follows.

8.2. Regarding Applicant's arguments on pages 21 - 22, section II., subsection D: The Applicant essentially recites sections of the specification that allegedly support the claim. The Examiner respectfully disagrees as follows: The Applicant's recited portions of the specification do not appear to support disassembling a binary code into a software simulation model. The specification

appears to teach disassembling binary code into an assembly code module. The Examiner remarks that deleting the phrase, "by disassembling a binary code" may overcome the rejection.

9. Regarding claim 33 rejected under 35 USC § 112, first paragraph:

9.1. Applicant's arguments have been fully considered, but are not persuasive, as follows.

9.2. Regarding Applicant's arguments on pages 23 - 25, section II., subsection E: The Applicant essentially recites sections of the specification that allegedly support the claim. The Examiner respectfully disagrees as follows: The Applicant's recited portions of the specification do not appear to support disassembling a binary code into a software simulation model. The specification appears to teach disassembling binary code into an assembly code module. The Examiner remarks that deleting the phrase, "by disassembling a binary code" may overcome the rejection.

10. Accordingly, the rejections are maintained.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

a. Claims 1 – 2, 4 – 22, 33 – 34, 36 - 60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in

such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

i. Regarding claim 41, the claim recites in lines 8 - 9, "generating a simulation model in a high level language format by disassembling a binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The invention does not appear to disassemble binary code into a simulation model as recited in the claim; rather, the specification appears to recite that binary code is disassembled into assembler, which is then provided to the translator (*specification, page 6, lines 7 – 8*).

ii. Regarding claim 41, the claim recites in lines 9 - 10, "wherein the software assembly code module comprises the binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The software assembly code module appears to be assembly code, rather than binary code.

iii. Regarding claim 55, the claim recites in lines 8 – 11, "processing … the data structure to refine accuracy of an assembler-level software simulation model by generating the assembler-level software simulation model based on the assembly language software module by using the assembly language software module or by *disassembling a binary code*". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s),

at the time the application was filed, had possession of the claimed invention. The invention does not appear to perform the recited process by disassembling a binary code; rather, the specification appears to recite that binary code is disassembled into assembler, which is then provided to the translator (*specification, page 6, lines 7 – 8*).

iv. Regarding claim 1, the claim recites in lines 12 – 13, "generating a software simulation model in a high level language format based at least in part upon the optimized assembler code by disassembling a binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. When a binary code is disassembled, the generated software simulation model does not appear to be based upon the assembler code that was created in the preceding limitations. Nor does disassembling a binary code appear to generate a software simulation model.

v. Regarding claim 9, the claim recites in lines 5 - 7, "generating a software simulation model in a high level language format by disassembling a binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The invention does not appear to disassemble binary code into a simulation model as recited in the claim; rather, the specification appears to recite that binary code is disassembled into assembler, which is then provided to the translator (*specification, page 6, lines 7 – 8*).

vi. Regarding claim 9, the claim recites in lines 7 - 8, "wherein the software assembly code module comprises the binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The software assembly code module appears to be assembly code, rather than binary code.

vii. Regarding claim 33, the claim recites in lines 13 - 14, "generating a software simulation model in a high level language format based at least in part upon the optimized assembler code by disassembling a binary code". This subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. When a binary code is disassembled, the generated software simulation model does not appear to be based upon the assembler code that was created in the preceding limitations. Nor does disassembling a binary code appear to generate a software simulation model.

viii. Regarding claim 61, the claim is rejected analogously to claim 1 above.

ix. Regarding claim 62, the claim is rejected analogously to claim 9 above.

x. Regarding claim 63, the claim is rejected analogously to claim 55 above.

xi. Regarding claim 64, the claim is rejected analogously to claim 55 above.

xii. Dependent claims inherit the defects of their parent claims.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12.1. Claims 41 - 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12.1.1. Regarding claim 41, the claim recites in lines 11, "the software simulation model". The term appears to have insufficient antecedent basis.

12.1.2. Regarding claim 41, the claim recites in lines 15 - 16, "the act of generating the software simulation model". The term appears to have insufficient antecedent basis.

12.1.3. Dependent claims inherit the defects of their parent claims.

Allowable Subject Matter

13. Claims 1 – 2, 4 – 22, 33 – 34 and 36 – 64 are allowable over the prior art of record.

14. Following is an Examiner's statement of reasons for indicating allowable subject matter.

15. The allowability of the claims resides, at least in part, that the closest prior art of record Bradford (U.S. Patent Number 5857093), Passerone ("Fast hardware/software

co-simulation for virtual prototyping and trade-off analysis"), Hellestrand (U.S. Patent Number 6230114), Zivojnovic ("Compiled HW/SW Co-simulation"), either alone or in combination with the prior art of record, do not teach or suggest a method for performing performance analysis for target machine, specifically including,

15.1. Regarding claim 1, "wherein the act of annotating the software simulation model is performed during a time of the act of generating the software simulation model", in combination with the remaining features and elements of the claimed invention,

15.2. Regarding claim 9, "wherein the act of annotating the software simulation model is performed during a time of the act of generating the software simulation model", in combination with the remaining features and elements of the claimed invention,

15.3. Regarding claim 33, "wherein the act of annotating the software simulation model is performed during a time of the act of generating the software simulation model", in combination with the remaining features and elements of the claimed invention,

15.4. Regarding claim 41, "wherein the act of annotating the software simulation model is performed during a time of the act of generating the software simulation model", in combination with the remaining features and elements of the claimed invention,

15.5. Regarding claim 55, "wherein the act of associating is performed during a time of the act of parsing the assembly language software into a data structure", in combination with the remaining features and elements of the claimed invention,

15.6. Regarding claim 61, "wherein the means for annotating the software simulation model is invoked during a time when the means for generating the software simulation model executes", in combination with the remaining features and elements of the claimed invention,

15.7. Regarding claim 62, "wherein the means for annotating the software simulation model is invoked during a time when the means for generating the software simulation model executes", in combination with the remaining features and elements of the claimed invention,

15.8. Regarding claim 63, "wherein the means for associating is invoked during a time when the means for parsing the assembly language software executes", in combination with the remaining features and elements of the claimed invention,

15.9. Regarding claim 64, "wherein the act of associating is performed during a time of the act of parsing the assembly language software into a data structure", in combination with the remaining features and elements of the claimed invention.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 10:00 AM - 6:30 PM.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123